39. (Amended) A pre-anneal intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:

a semiconductor substrate having a first surface and a second surface;

at least one first doped area on said substrate first surface;

at least one second, differently doped area within said at least one first doped area; and

a substantially dopant-free, uninterrupted diffusion barrier layer extending over said [at least one first doped area on said substrate] first surface and said second surface of said semiconductor substrate.

Please cancel claims 41 and 42 without prejudice or disclaimer.

REMARKS

This amendment is in response to the Advisory Action mailed June 27, 2000 (hereinafter "the Advisory Action"), which has been received and reviewed. It is noted in the Advisory Action that the amendments proposed in the Amendment Under 37 C.F.R. § 1.116, mailed by applicants on June 19, 2000, were not entered because they were not "deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal." It is further stated in the Advisory Action that applicants "request for reconsideration has been considered but does not place the application in condition for allowance because . . . the arguments are directed to the references [cited in the Final Office Action mailed April 19, 2000] individually. Where appropriate, applicants have herein modified the arguments included in the previous unentered Amendment Under 37 C.F.R. § 1.116 in order to more clearly address the combined teachings of references cited in the Final Office Action mailed April 19, 2000 (hereinafter "the Office Action"). Therefore, applicants respectfully request reconsideration of the application in light of the amendments and revised remarks contained herein.

Each of claims 25 through 28 and 31 through 45 are rejected in the Office Action under 35 U.S.C. § 102(b) or 35 U.S.C. § 103(a). However, applicants have herein canceled claims 27,

28, 35, 36, 41, and 42 without prejudice or disclaimer. Further, applicants have herein amended claims 25, 33, and 39, and, after careful consideration of the teachings of the references cited in the Office Action, applicants respectfully submit that claims 25, 26, 31 through 34, 37 through 40, and 43 through 45 recite subject matter which is novel and nonobvious in light of the references cited in the Office Action.

Entry of Amendments

The amendments to the claims are supported by the application as filed, and entry thereof is respectfully solicited. No new matter has been added.

35 U.S.C. § 102(b) Anticipation Rejections

Claims 25, 26, 31, 33, 34, 37 through 40, 43, and 45 stand rejected under 35 U.S.C. § 102(b) (hereinafter "Section 102(b)) as being anticipated by Tada (U.S. Patent No. 5,545,577). In order for a claim to be anticipated under Section 102(b), each and every element as set forth in the claim must be expressly or inherently described in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in the allegedly anticipating reference in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). However, applicants respectfully submit that Tada does not expressly or inherently teach each and every limitation of any one of claims 25, 26, 31, 33, 34, 37 through 40, 43, or 45, particularly when the amendments to claims 25, 33, and 39 are considered. Thus, applicants respectfully request that rejections of claims 25, 26, 31, 33, 34, 37 through 40, 43, and 45 under Section 102(b) in light of Tada be withdrawn.

As they are amended, claims 25, 33, and 39 are each independent claims reciting a "pre-anneal intermediate structure in the formation of an isolation structure for a semiconductor device." The intermediate structures of amended claims 25, 33, and 39 each include a semiconductor substrate with first and second surfaces, as well as a substantially dopant-free, uninterrupted diffusion barrier layer extending over the first and second surfaces of the semiconductor substrate.

Though each of claims 25, 33, and 39 also include various other limitations, a reference can not anticipate any one of amended claims 25, 33, or 39, unless that reference explicitly or inherently teaches a structure including a semiconductor substrate having first and second surfaces, as well as a substantially dopant-free, uninterrupted diffusion barrier layer extending over the first and second surfaces of the semiconductor substrate. *See, Richardson*, 9 USPQ2d 1913 (Fed. Cir. 1989).

Claims 26, 31, 34, 37, 38, 40, 43, and 45 are all dependent claims: claims 26 and 31 depend from claim 25; claims 34, 37, and 38 depend from claim 33; and claims 40, 43, and 45 depend from claim 39. As such, each of claims 26, 31, 34, 37, 38, 40, 43, and 45 incorporates every limitation recited in the independent claim from which it depends. Therefore, in order to anticipate claims 26, 31, 34, 37, 38, 40, 43, and 45, a reference must at least expressly or inherently teach every limitation recited in claim 25, claim 33, and claim 39, as each is amended.

Applicants respectfully submit that Tada does not expressly or inherently teach the limitations recited in any one of amended claims 25, 33, or 39. Specifically, as is noted in the Office Action, Tada does not teach a pre-anneal intermediate structure including a semiconductor substrate having first and second surfaces and a substantially dopant-free, uninterrupted diffusion barrier layer extending over the first and second surfaces of the semiconductor substrate (*See, Office Action*, page 4). Consequently, applicants respectfully submit that Tada does not anticipate claims 25, 33, and 39, as they are amended. Moreover, because Tada does not expressly or inherently teach every limitation recited in any one of claims 25, 33, or 39, applicants further submit that Tada can not anticipate claims 26, 31, 34, 37, 38, 40, 43, and 45, each of which depends from claim 25, claim 33, or claim 39. Therefore, applicants respectfully request that the rejections of claims 25, 26, 31, 33, 34, 37 through 40, 43, and 45 under Section 102(b) be withdrawn.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,545,577 to Tada and Further in View of U.S. Patent No. 5,837,378 to Mathews et al.

Claims 27, 28, 35, 36, 41, and 42 stand rejected under 35 U.S.C. § 103(a) (hereinafter "Section 103(a)") as being unpatentable over Tada (U.S. Patent No. 5,545,577), as applied to claims 25 and 34 above, and further in view of Mathews et al. (U.S. Patent No. 5,837,378).

However, applicants respectfully submit that each of these rejected claims are canceled herein without prejudice or disclaimer. Therefore, applicants respectfully submit that the rejection of claims 27, 28, 35, 36, 41, and 42 is no longer relevant, and applicants respectfully request that it be withdrawn.

Though claims 27, 35, and 41 have been canceled without prejudice or disclaimer, applicants respectfully note that the limitations recited in claims 27, 35, and 41 have generally been incorporated into amended claims 25, 33, and 39, respectively. However, applicants respectfully submit that combined teachings of Tada and Mathews et al. do not render amended claims 25, 33, and 39 obvious under Section 103(a).

As is set forth in M.P.E.P § 706.02(j), three essential criteria must be met before a *prima facie* case of obviousness can be properly established.

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Significantly, the combined teachings of Tada and Mathews et al. would not motivate one of ordinary skill in the art to modify the combined teachings of the references to arrive at the structures recited in claims 25, 33, and 39, as they are amended. Moreover, the combined teachings of Tada and Mathews et al. do not teach or suggest all of the limitations recited in claims 25, 33, and 39, as they are amended. Therefore, applicants respectfully submit that the combination of Tada and Mathews et al. can not establish the *prima facie* obviousness of these claims

Amended Claims 25, 33, and 39 each recite pre-anneal intermediate structures. The intermediate structures of claims 25, 33, and 39, as amended, include a semiconductor substrate having a first surface and a second surface, at least one doped area on the first surface of the semiconductor substrate, and a substantially dopant-free, uninterrupted diffusion barrier layer extending over the first and second surfaces of the semiconductor substrate. Therefore, before

claims 25, 33, and 39 can be shown to be *prima facie* obvious in light of the combination of Tada and Mathews et al., it must be shown that the combined teachings of Tada and Mathews et al. teach or suggest each of these limitations and that one of ordinary skill in the art would be suggested or motivated to combine the teachings of Tada and Mathews et al. to arrive at a structure having such characteristics.

First, Tada does not teach or suggest an intermediate structure as recited in any one of claims 25, 33, or 39, as they are amended. Specifically, Tada does not teach an intermediate structure including a semiconductor substrate having first and second surfaces, at least one doped area on the substrate first surface, and a substantially dopant-free, uninterrupted diffusion barrier layer extending over the first and second surfaces of the semiconductor substrate. Moreover, the teachings of Tada do not suggest the fabrication of such an intermediate structure or its attendant advantages. Thus, Tada fails to teach or suggest an intermediate structure having all the limitations of any one of the structures defined by claims 25, 33, or 39, as amended.

Second, combining the teachings of Mathews et al. with the teachings of Tada does not remedy the deficiencies of Tada. Mathews et al. teaches a method of reducing stress-induced defects in silicon. During the course of the process taught by Mathews et al., an intermediate structure is created which includes a "masking stack" (an oxide layer and a nitride layer) on both the top and bottom surfaces of a silicon wafer. Significantly, the masking stack of Mathews et al. is not a diffusion barrier layer, and Mathews et al. does not teach or suggest formation of such a masking stack over a semiconductor substrate having even one doped area.

The masking stack formed in the method of Mathews et al. is formed over a semiconductor substrate before any doped regions or isolation regions are formed over the semiconductor substrate (*See, Mathews et al.*, FIG. 2A through FIG. 2g). According to the teachings of Mathews et al., the nitride and oxide layers of the portion of the masking stack overlying the upper surface of the semiconductor substrate are used to form isolation regions in subsequent process steps. However, Mathews et al. teaches that the portion of the masking stack formed over the bottom surface of the semiconductor substrate must be removed before further process steps are executed (*See, Id.*, col. 2, lines 15-22, col. 5, lines 31-41, and col. 6, lines 12-16), thereby compromising or interrupting the

masking stack before any isolation structures or doped regions are formed. Moreover, the portion of the masking stack formed over the top portion of the semiconductor substrate in the method of Mathews et al. is at least partially etched during the subsequent formation of isolation regions and before any doped regions are formed in the semiconductor substrate (*See, Id.*, col. 2, lines 15-58, col. 5, lines 31-67, col. 6, lines 1-11, FIG. 2A through FIG. 2G). Applicants respectfully submit that the masking stack of Mathews et al. could not prevent the out-diffusion dopants during an anneal step and is not a substantially dopant-free, uninterrupted diffusion barrier layer as recited in claims 25, 33, and 39 because the masking stack is nearly entirely compromised before any implantation steps occur. Therefore, even the combined teachings of Tada and Mathews et al. fail to teach or suggest a an intermediate structure including a semiconductor substrate having first and second surfaces, at least one doped area on the substrate first surface, and a substantially dopant-free, uninterrupted diffusion barrier layer extending over the first and second surfaces of the semiconductor substrate

In addition, applicants respectfully submit that the ordinarily skilled artisan would have no motivation to combine or modify the teachings of Tada and Mathews et al. to arrive at the intermediate structures recited in amended claims 25, 33, and 39, especially if the teachings of Mathews et al. are considered. It is stated in the Office Action that "[i]t would have been obvious to one having ordinary skill in the art . . . to form the barrier layer (154b) over second surface of the substrate (100) of Tada as taught by Mathews because the formation of the substantially dopant-free, uninterrupted diffusion barrier layer on the second surface reduces overall stress on the wafer thus prevent[ing] warpage" (*Office Action*, page 6). Applicants respectfully submit, however, that this assertion ignores the fact that Mathews et al. teaches only a method for reducing stress while forming a field oxide pattern on a semiconductor substrate **before** any doping of the semiconductor substrate is performed. In fact, Mathews et al. repeatedly teaches that failure to remove the portion of the masking stack formed on the bottom surface of the semiconductor substrate before further processing significantly increases the likelihood of stress-induced defects in the subsequently completed semiconductor device (*See, Mathews et al.*, col. 2, lines 15-67, col. 4, lines 31-67, and col. 5 through col. 6). Thus, Mathews et al. teaches strongly away from the structures recited in amended claims 25, 33, and 39. Moreover, neither Mathews et al. nor Tada provide any teaching or suggestion that might reveal the desirability of forming the intermediate structures recited in amended claims 25,

33, and 39, and no other motivation to combine the teachings of Tada and Mathews et al. has been provided in the Office Action. As a consequence, applicants respectfully submit that the combination of Tada and Matthews can not establish the *prima facie* obviousness of amended claims 25, 33, and 39. The combined teachings of these references could only motivate one of ordinary skill in the art not to form the intermediate structures recited in claims 25, 33, and 39, as they are amended.

Applicants respectfully submit that each of the claims now pending in the application recite subject matter which is non-obvious in light of the combined teachings of Tada and Mathews et al. As is detailed herein, the combination of Tada and Mathews et al. does not render amended claims 25, 33, and 39 *prima facie* obvious, and each of remaining claims 26, 31, 34, 37, 38, 40, 43, and 45 depends from claim 25, claim 33, or claim 39. Therefore, because a dependent claim can only be obvious if the independent claim from which it depends is obvious, applicants respectfully submit that each of the claims now pending in the application are patentable over the combination of Tada and Mathews et al. *See, In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988); M.P.E.P. § 2143.03.

Obviousness Rejection Based on U.S. Patent No. 5,545,577 to Tada and Further in View of U.S. Patent No. 5,846,596 to Shim et al.

Claim 32 stands rejected under Section 103(a) as being unpatentable over Tada and further in view of Shim et al. (U.S. Patent No. 5,846,596). However, applicants respectfully submit that the combined teachings of Tada and Shim et al. do not establish the *prima facie* obviousness of claim 32. Thus, applicants respectfully traverse the rejection of claim 32 under Section 103(a) and request that this rejection be withdrawn.

As was already detailed, a *prima facie* case of obviousness can not be properly established unless the combined prior art references teach or suggest all the limitations of the claims rejected. Claim 32 depends from amended claim 25. Consequently, the pre-anneal structure recited in claim 32 includes a semiconductor substrate having a first surface and a second surface, at least one p-well and at least one n-well on the substrate first surface, at least one p-type area within the at least one n-well, at least one n-type area within the at least one p-well, and a substantially dopant-free, uninterrupted diffusion barrier layer extending over the first and second surfaces of the semiconductor substrate. The teachings of Tada combined with the teachings of Shim et al. simply

do not teach or suggest an intermediate structure having each of these limitations. Thus, applicants respectfully submit that the combination of references cited against claim 32 does not support a *prima facie* case of obviousness.

As already discussed herein, Tada does not teach or suggest a pre-anneal intermediate structure including a semiconductor substrate having a first surface and a second surface, at least one p-well and at least one n-well on the substrate first surface, at least one p-type area within the at least one n-well, at least one n-type area within the at least one p-well, and a substantially dopant-free, uninterrupted diffusion barrier layer extending over the first and second surfaces of the semiconductor substrate. Specifically, as is highlighted in the Office Action, Tada does not teach a pre-anneal intermediate structure including a semiconductor substrate having one or more doped regions as well as a diffusion barrier layer extending over the top and bottom surfaces of the semiconductor substrate (*See, Office Action,* page 4).

Significantly, combining the teachings of Shim et al. with the teachings of Tada does not correct the shortcomings of Tada. Shim et al. teaches a method of forming field oxide isolation regions having sloped edges. During the process taught by Shim, oxide layers and non-oxidative nitride layers are formed over the semiconductor substrate surface. However, Shim et al. does not teach extending a diffusion barrier layer over first and second surfaces of a doped semiconductor substrate included in a pre-anneal intermediate structure. In fact, Shim et al. teaches only a method of creating a field oxide structure which defines areas on the surface of a semiconductor substrate which are to be **subsequently** doped (*See, Shim et al.*, col. 3, lines 26-32). Moreover, Shim et al. is devoid of any teaching or suggestion that would motivate one of ordinary skill in the art to form a diffusion barrier layer over the semiconductor substrate before an annealing step. Thus, applicants respectfully submit that the combined teachings of Tada and Shim et al. do not teach or suggest each of the limitations recited in claim 32, and applicants respectfully request that the rejection of claim 32 under Section 103(a) as unpatentable over Tada combined with Shim et al. be withdrawn.

Drawings

Applicants will file corrected formal drawings upon receipt of a Notice of Allowance and Issue Fee Due in the application.

CONCLUSION

Claims 25, 26, 31 through 34, 37 through 40, and 43 through 45 are believed to be in condition for allowance. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

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